Listing of Claims

The following listing of claims replaces all prior versions.

1. (Currently amended) An integrated circuit comprising:

a plurality of serializer/deserializers (SERDESs);

core processing logic integrated with each said SERDES and connected to each said SERDES to exchange signals therewith; and

a plurality of functionally identical testers integrated with said plurality of SERDESs and said core processing logic, said testers being connected to individually test each said SERDES, each of said testers being enabled to detect performance characteristics of individual said SERDESs independently of other said testers and concurrently with said plurality of SERDESs, wherein a bit error rate for each said SERDES is individually identified;

wherein each said tester is connected to a common test bus that is integrated with said SERDESs and said testers, said common test bus being separate from a data bus, each said tester having a unique address that enables independent accessibility of said tester via said test bus, said test bus being dedicated to providing signaling for said enablement to detect performance characteristics of said individual SERDESs and further comprising a built in self-test (BIST) state machine integrated with said SERDESs and said testers, said BIST being connected to said test bus and being configured to sequence test operations by said individual said testers.

2. (Original) The integrated circuit of claim 1 further comprising a semiconductor substrate on which said SERDESs, said core processing logic and said testers are fabricated.

3. (Original) The integrated circuit of claim 1 wherein each said tester includes a test controller and a test interface, each said tester being dedicated to a specific said SERDES, said test interface of each said tester being coupled between said core processing logic and said SERDES to which said each tester is dedicated, said tester controller being configured to select among a normal operation mode and a plurality of test modes for operation of said test interface.

4. (Original) The integrated circuit of claim 3 wherein each said test interface includes a test pattern generator that is connected to inputs of parallel data of said SERDES to which said test interface is dedicated, said test interface further including an error detector connected to outputs of parallel data from said SERDES.

5. (Canceled)

6. (Previously presented) The integrated circuit of claim 1 further comprising an input/output tester controller integrated with said SERDESs and said testers, said input/output tester controller being coupled between said test bus and an output of said integrated circuit for signal communication with an external source for sequencing test operations.

7. (Canceled)

8. (Original) The integrated circuit of claim 1 wherein said testers are responsive to individual commands and are configured to be individually but concurrently operated, said testers having a one-to-one correspondence with said SERDESs.

9. (Currently amended)) An integrated circuit comprising:

a single semiconductor substrate onto which integrated circuitry is fabricated;

core circuitry integrated onto said substrate;

a plurality of SERDESs integrated onto said substrate, each said SERDES having parallel data inputs and parallel data outputs and having serial data inputs and outputs;

a plurality of functional test interfaces (FTIs) integrally formed with said substrate, each said FTI being uniquely associated with one of said SERDESs and being connected to said parallel data inputs and outputs of said associated SERDES, said FTIs being enabled to individually and concurrently test performances of said SERDESs wherein a bit error rate for each said SERDES is individually identified;

a plurality of functional test controllers (FTCs) integrally formed with said substrate, each said FTC being uniquely associated with one of said FTIs and being

configured to select among operational modes of said associated FTI; and

an input/output controller (IOC) and common test bus integrally formed with said substrate, said common test bus being dedicated to providing signaling for enablement of testing, said common test bus being separate from a data bus, said IOC being connected to each said FTC via said common test bus to transmit individually addressed commands to each said FTC, said IOC further being connected to exchange signals with an external device.

10. (Original) The integrated circuit of claim 9 wherein each said FTI is configured to operate in a plurality of alternative said operational modes, including a normal-operation mode in which data is transmitted between said core circuitry and said associated SERDES via said FTI.

11. (Original) The integrated circuit of claim 9 wherein each said FTI includes a pattern generator connected to said parallel data inputs of said associated SERDES and includes an error detector connected to said parallel data outputs of said associated SERDES.

12. (Original) The integrated circuit of claim 9 further comprising a built-in-self-tester (BIST) integrally formed on said substrate, said BIST being connected and configured to activate testing via said FTIs.

13. (Original) The integrated circuit of claim 9 wherein each of said FTIs is connected to said IOC via a common test bus, said FTIs also being connected to said core circuitry.

14. (Original) The integrated circuit of claim 13 wherein each said FTI is assigned a unique address, said IOC being enabled to individually manipulate said FTIs by employing said unique addresses.

15. (Currently amended) A method of testing operations of serializer/deserializers (SERDESs) of an integrated circuit comprising the steps of:

embedding a plurality of test interfaces within said integrated circuit such that each test interface is specific to one said SERDES with respect to exchanging parallel data,

including forming each said test interface to include a test pattern generator connected to parallel data inputs of said SERDES to which said test interface is specific and further including forming each said test interface to include an error detector to receive parallel data from said SERDES to which said test interface is specific, wherein each of a plurality of SERDESs is individually and concurrently tested and a bit error rate of each said SERDES is individually identified;

embedding test controllers within said integrated circuit such that each said test controller is specific to one said test interface with respect to triggering test operations by said test interface;

providing an integrated circuit output that enables said test controllers to be individually addressed; and

embedding an input/output controller (IOC) and a test bus within said integrated circuit, including connecting said IOC between said integrated circuit output and said test bus and including linking each said test controller to said test bus, said test bus being separate from a data bus.

16. (Canceled)

17. (Original) The method of claim 15 further comprising a step of concurrently enabling all of said test interfaces to simultaneously monitor performances of said SERDESs.

18. (Original) The method of claim 15 further comprising the step of embedding a built-in-self-test (BIST) state machine within said integrated circuit such that said BIST is connected to each said test controller.

19. (Original) The method of claim 15 further comprising the step of forming an insulative package to house circuitry of said integrated circuit.

20. (Canceled)